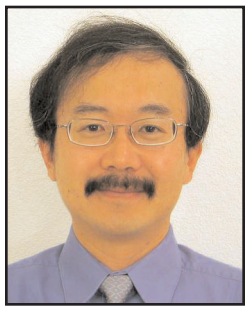
Session 14 Overview

Baseband and Channel Processing



Chair: K. Lawrence Loh, MediaTek, Hsinchu City, Taiwan

Associate Chair: Steffen Paul, Infineon, Munich, Germany

Silicon implementations based on DSP technologies continue to advance in both wireless communications and mass storage applications. This session provides a snapshot of advances in baseband and channel signal processing to provide economic and power-saving solutions in cellular feature phones, UWB and digital TV applications. Important digital communication building blocks, including an all-digital spread-spectrum clock generator, and direct digital frequency synthesizer/mixer technologies, are presented to mark the increased performance as well as power efficiency. In the mass storage area, the session reports a variety of highly-integrated SoC solutions to target read/write operations of multiple formats of existing and emerging optical disks.

In Paper 14.1 a mixed-signal 90nm GSM/EDGE baseband processor featuring multimedia enhancements and low power features is presented. Supply gating and dynamic voltage/frequency scaling are used to minimize both the leakage and dynamic power consumption in a given application scenario. A power metric of 0.47mW/MHz is reported.

The authors of Paper 14.2 report on an all-digital spread spectrum clock generator for reducing electromagnetic interference by over 13dB. Their solution is capable of spreading the clock power spectrum both upwards and downwards using a very power/area efficient digital-delay-line-based approach that consumes 7.1mW of power and 0.06mm^2 in 0.15µm CMOS.

Two very different approaches for implementing direct digital frequency synthesizers (DDFS) are presented in Papers 14.3 and 14.4. The first paper describes a new multipartite table-based approach that achieves an SFDR of over 90dBc at a clock frequency of 630MHz, a power dissipation of 76mW, and a frequency resolution of 0.15Hz. The second paper integrates a mixer with a DDFS delivering an SFDR over 90dBc, generating 13-bit quadrature outputs. This integrated solution consumes 150mW at 380MHz.

A contribution to DSSS UWB digital transceivers is presented in Paper 14.5. The proposed solution targets ad-hoc wireless mesh networks, providing fast acquisiton (< 8µs), and a ±7.5cm ranging accuracy. Power saving features allow a 4 to 25x reduction in power consumption.

A COFDM receiver supporting DVB-T/H is described in Paper 14.6. It features a 2D linear equalizer, allowing it to overcome a 70Hz Doppler frequency shift. Data rates up to 31.67Mb/s are supported at a power consumption of 250mW.

In Paper 14.7, a 0.13µm read/write channel SoC for all formats of both conventional (CD/DVD) and emerging (HD-DVD/BD) optical disks is integrated with dual processors to assist servo controls and I/O operations. Data rates up to 550Mb/s on the read PRML channel are supported, and a power consumption of 2.7W is reported for a 16x DVD playback.

A highly-integrated mixed-signal SoC for all existing commercial optical storage formats is presented in Paper 14.8. An aggressive power management scheme enables the inclusion of all major functional blocks in a single chip for full-format optical drives including read/write channels, servo controls, 4-LVDS channel write strategies generator, and a 1.5Gb/s serial-ATA PHY.

14.1 A 90nm CMOS Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor with 380MHz ARM9 Core and Mixed-Signal Extensions **8:30 AM**

T. Lüftner, Infineon, Munich, Germany

A 43.56mm² GSM/EDGE baseband processor in 90nm triple-well CMOS has multi-media and mixed-signal extensions, including a 16b HiFi audio front end. The ARM9 core with thin-gate devices reaches 380MHz operation at 470µW/MHz. Frequency and voltage scaling reduce active power in slow mode by 40% and there are nine independent power domains.

14.2 All-Digital Spread Spectrum Clock Generator for EMI Reduction **9:00 AM**

S. Damphousse, ESS Technology, Kelowna, Canada

An all-digital spread spectrum clock generator is presented. A digital delay matrix (DDM) is used to adjust the delay on a clock, modulating the output and producing an up or down spread. The DDM delay is no longer than one period of the clock. Measured peak clock power reduction is greater than 13dB. The circuit occupies 0.06mm² in a 0.15µm CMOS process and consumes 7.1mW.

14.3 A 630MHz Direct Digital Frequency Synthesizer with 90dB SFDR in 0.25µm CMOS **9:30 AM**

D. De Caro, University of Naples, Naples, Italy

Multipartite table methods are used in the implementation of a direct digital frequency synthesizer. Two quadrature 13b outputs are produced with a SFDR >90dB and a frequency resolution of 0.15Hz at a 630MHz clock frequency. The 0.25µm CMOS chip occupies 0.063mm² and dissipates 76mW from a 2.5V supply at 630MHz.

14.4 A 380MHz 150mW Direct Digital Synthesizer/Mixer in 0.25µm CMOS **9:45 AM**

D. De Caro, University of Naples, Naples, Italy

A direct digital frequency synthesizer/mixer IC processes two 12b quadrature inputs by providing two quadrature 13b outputs with a SFDR greater than 90dB and a frequency resolution of 0.088Hz at 380MHz clock frequency. The IC has an area of 0.22mm² in 0.25µm CMOS and dissipates 150mW at 380MHz with a supply of 2.5V. At 1.8V, the power dissipation is 53mW at 270MHz.

14.5 A DSSS UWB Digital PHY/MAC Transceiver for Wireless Ad-Hoc Mesh Networks with Distributed Control **10:15 AM**

A. Koyama, Sony, Tokyo, Japan

A DSSS UWB digital PHY/MAC transceiver with distributed control has been developed. This chip provides fast acquisition within 8µs and ±7.5cm ranging accuracy, as well as distributed wireless access control of up to 64 terminals and a power save control function. Die area is 12.2mm² in a 0.13µm CMOS process. The maximum power dissipation of the core is 181mW at 1.2V.

14.6 A 1.8V 250mW COFDM Baseband Receiver for DVB-T/H Applications **10:45 AM**

L-F. Chen, National Chiao Tung University, Hsinchu, Taiwan

A DVB-T/H baseband receiver with multi-stage power control, 2D linear channel equalizer, synchronizer, 2/4/8k-point FFT, and Viterbi/RS decoder is implemented in 0.18µm CMOS. At the highest data rate of 31.67Mb/s, it overcomes 70Hz Doppler frequency and consumes 250mW with a die size of 6.9×5.8mm².

14.7 A 0.13µm CMOS SoC for All-Format Blue and Red Laser DVD Front-End Digital Signal Processing **11:15 AM**

M. Bathaee, Atmel, San Jose, CA

This paper presents an all-format DVD SoC front-end DSP capable of 550Mb/s for HD-DVD, Blu-ray disc and DVD/CD red laser rewritable standards. This chip includes an analog front-end, PRML read channel, disc controller, servo system and dual processor. The analog blocks contain 640k transistors, and the digital blocks consist of 2.3M gates with a die area of 62mm².

14.8 Fully Integrated CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications with On-Chip 4-LVDS Channel WSG and 1.5Gb/s SATA PHY **11:45 AM**

B-Y. Hsieh, MediaTek, Hsin-Chu City, Taiwan

Multi-format CD/DVD SoC, integrating an RF/AFE and a 1.5Gb/s SATA PHY, is presented. It supports a 471Mb/s 18x DVD. A partial parity mode reduces SDRAM bandwidth and a power control mode minimizes the system clock rate. The 0.18µm CMOS SoC has 10M transistors, occupies 5.4×5.1mm², and consumes 772mW during a 16x DVD read.